

[Sign in](#)
[Web](#)
[Images](#)
[Video](#)
[News](#)
[Maps](#)
[more »](#)

branch target address cache

Search

[Advanced Search](#)  
[Preferences](#)

Web

Results 1 - 10 of about 1,270,000 for branch target address cache. (0.25 seconds)**Evaluation of a branch target address cache**

Branches interrupt the sequential flow of instructions and introduce pipeline bubbles.

**Branch** penalty can be a significant component of effective cpi ...

csdl.computer.org/comp/proceedings/hicss/1995/6930/00/69300173abs.htm -

[Similar pages](#)**[PDF] Evaluation of a Branch Target Address Cache**

File Format: PDF/Adobe Acrobat

cache sizes on the efficiency of **branch target address** ... 2 The **Branch Target****Address Cache**. Condition codes in 4s are single bits in a 64-bit Condi- ...csdl.computer.org/comp/proceedings/hicss/1995/6930/00/69300173.pdf - [Similar pages](#)**Branch target predictor - Wikipedia, the free encyclopedia**In more parallel processor designs, as the instruction **cache** latency grows longer and the fetch width grows wider, **branch target** extraction becomes a ...en.wikipedia.org/wiki/**Branch\_target\_predictor** - 12k - [Cached](#) - [Similar pages](#)**Welcome to IEEE Xplore 2.0: Evaluation of a branch target address ...**We discuss the impact of different **branch target caching** policies and **cache** sizes on the efficiency of **branch target address cache**. ...ieeexplore.ieee.org/xpls/abs\_all.jsp?arnumber=375396 - [Similar pages](#)**[PDF] Evaluation of a branch target address cache - System Sciences. Vol ...**

File Format: PDF/Adobe Acrobat

Page 1. Page 2. Page 3. Page 4. Page 5. Page 6. Page 7. Page 8.

ieeexplore.ieee.org/iel2/3016/8568/00375396.pdf?arnumber=375396 - [Similar pages](#)[ [More results from ieeexplore.ieee.org](#) ]**Data processor with branch target address cache and method of ...**A data processor (10) has a BTAC (48) storing a number of recently encountered fetch **address-target address** pairs. Each pair also includes an offset tag ...www.freepatentsonline.com/5530825.html - 71k - [Cached](#) - [Similar pages](#)**Pipelined two-cycle branch target address cache - Patent 6279105**In a **branch** instruction **target address cache**, an entry associated with a fetched block of instructions includes a **target address** of a **branch** instruction ...www.freepatentsonline.com/6279105.html - 51k - [Cached](#) - [Similar pages](#)**Branch-Target Buffer or Branch-Target Address Cache**Variations: **Branch Target Cache** (BTC): stores one or more **target** instructions additionally. Return **Address Stack** (RAS): a small stack of return addresses ...csdl.ijs.si/courses/processor/Chapter4/tlsd026.htm - 2k - [Cached](#) - [Similar pages](#)**Branch-Target Buffer or Branch-Target Address Cache**

First ...

csd.ijs.si/courses/processor/Chapter4/sld027.htm - 2k - [Cached](#) - [Similar pages](#)

### Prediction and Profile Buffers -- Mark Smotherman

BHT yes **branch** history table BPC tags yes yes yes **branch** prediction cache BTAC tags yes **branch target address cache** BTB tags yes yes **branch target** buffer ...  
www.cs.clemson.edu/~mark/predict.html - 14k - [Cached](#) - [Similar pages](#)

Google

Result Page:    1   2   3   4   5   6   7   8   9   10    [Next](#)

Free! Get the Google Toolbar. [Download Now](#) - [About Toolbar](#)

Google	<input type="text"/>	<input type="button" value="C Search"/>	<input type="button" value="PageRank"/>	<input type="button" value="Check"/>	<input type="button" value="Autolink"/>	<input type="button" value="Autofill"/>	<input type="button" value="Options"/>	<input type="button" value="Highlight"/>
--------	----------------------	---	---	--------------------------------------	---	---	--	--

---

branch target address cache	<input type="button" value="Search"/>
-----------------------------	---------------------------------------

[Search within results](#) | [Language Tools](#) | [Search Tips](#) | [Dissatisfied? Help us improve](#)

---

[Google Home](#) - [Advertising Programs](#) - [Business Solutions](#) - [About Google](#)

©2006 Google



register relative btac i/o

Search

[Advanced Scholar Search](#)[Scholar Preferences](#)[Scholar Help](#)

**Scholar** [All articles](#) [Recent articles](#) Results 1 - 10 of about 25 for register relative btac i/o. (0.21 seconds)

**All Results**[A Scott](#)[A Gara](#)[D Hunt](#)[T Ungerer](#)[K Burkhart](#)

[Development of Processor Cores for Digital Consumer Appliances - group of 2 »](#)  
F Arakawa, T Yamada, T Okada, M Ishikawa, Y Kondo, ... - Systems and Computers in Japan, 2006 - doi.wiley.com

... which is the reason we did not adopt **BTAC** architecture. ... 6. Middleware **relative** performance of SH-X. ... an example of the clock activity control of a **register** file ...  
[Related Articles](#) - [Web Search](#)

[Access type, memory system design, 108–109 Accumulator-based processor assembly language ...](#)  
ARM ARM - Architecture - doi.wiley.com  
... mode, 23 indirect mode, 22 **relative** mode, 23 ... floating-point representation, 75 Base **register** sets, X86 ... 207 Branch target address cache (**BTAC**), pipeline stall ...  
[Web Search](#)

[Four-Way Superscalar PA-RISC Processors - group of 9 »](#)  
AP Scott, KP Burkhart, A Kumar, RM Blumberg, GL ... - Hewlett-Packard Journal, 1997 - docencia.ac.upc.edu  
... If a branch hits in the **BTAC** but is predicted not ... its result is held in a temporary rename **register** and made ... **Relative** to the PA 7200, the misprediction rate is ...  
[Cited by 20](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#) - [BL Direct](#)

[PC Processor Microarchitecture - group of 31 »](#)  
K Diefendorff - Microdesign Resources, Microprocessor Report, 1999 - ece.umd.edu  
... Instead of a **BTAC**, some processors use a branch target instruction cache ... **Register** File ... however. Designed as shared multidrop buses for DRAM, I/O, and multiproces ...  
[Cited by 2](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

[On Speculation Control in Simultaneous Multithreaded Processors - group of 2 »](#)  
U Sigmund, T Ungerer - Journal of Universal Computer Science, 2001 - jucs.org  
... thread executes in a separate architectural **register** set. ... thread); a 1024-entry branch target address cache (**BTAC**); ... in Figure 15 and the **relative** IPC decrease ...  
[Cited by 1](#) - [Related Articles](#) - [Web Search](#)

[Overview of the Blue Gene/L system architecture - group of 4 »](#)  
A Gara, MA Blumrich, D Chen, GLT Chiu, P Coteus, ... - IBM Journal of Research and Development, 2005 - research.ibm.com  
... A branch target address cache (**BTAC**) reduces branch latency. ... each with its own arithmetic pipe and **register** file ... The **relative** size of the sections is adjustable ...  
[Cited by 27](#) - [Related Articles](#) - [Cached](#) - [Web Search](#)

[Advanced performance features of the 64-bit PA-8000 - group of 3 »](#)  
D Hunt - Compcon'95. Technologies for the Information Superhighway, ..., 1995 - ieeeexplore.ieee.org  
... As men- tioned earlier, the **BTAC** avoids the taken branch ... bus, Store data is copied from the **register** file to the ... Loads and stores to the I/O address space and ...  
[Cited by 104](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

Mispredicted Path Cache Effects

P Amestoy... - Springer

... associative branch target address cache (BTAC) and a ... of mispredicted path execution while enforcing **register** and memory ... a function of the **relative** frequency of ...

[Related Articles](#) - [Web Search](#)Permeability characteristics of lipid bilayers from lipoic acid-derived phosphatidylcholines. ... - group of 2 »

J Stefely, MA Markowitz, SL Regen - Journal of the American Chemical Society, 1988 - pubs.acs.org

... It is also not obvious whether polymerized bilayers should be more or less permeable **relative** to their monomeric counterparts. ... CB 1 n | | o=c c=o | | CH3 ...

[Cited by 4](#) - [Related Articles](#) - [Web Search](#)Exploring the design space of LUT-based transparent accelerators - group of 6 »

S Yehia, N Clark, S Mahlke - Proceedings of the 2005 international conference on ..., 2005 - portal.acm.org

... a BRL has an entry in the BTAC, control is ... variety of sub- graphs, while maintaining a **relative** low interconnect ... 2. Each bit of the output **register**, r7, can be ...

[Cited by 1](#) - [Related Articles](#) - [Web Search](#)

Google ►

Result Page: 1 2 3 [Next](#)[Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2006 Google



**Search Results**      **BROWSE**      **SEARCH**      **IEEE XPLORE GUIDE**      **SUPPORT**

Results for "( ( btac<in>metadata ) <and> ( relative<in>metadata ) )<and> ( i/o<in>..."  
Your search matched 0 documents.  
A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.



» Search Options

[View Session History](#)

[New Search](#)

Modify Search

(( ( btac<in>metadata ) <and> ( relative<in>metadata ) )<and> ( i/o<in>metadata )



☐ Check to search only within this results set

Display Format:    ☒ Citation    ☐ Citation & Abstract

» Key

 Indicates full text access

- IEEE JNL    IEEE Journal or Magazine
- IEE JNL    IEE Journal or Magazine
- IEEE CNF    IEEE Conference Proceeding
- IEE CNF    IEE Conference Proceeding
- IEEE STD    IEEE Standard

No results were found.  
Please edit your search criteria and try again. Refer to the Help pages if you need assistance revising your search.

